AMENDMENT TO THE SPECIFICATION

Please replace the paragraph beginning on page 7, line 19, with the following amended paragraph:

If a transparent path exists for the path L1-L2-L4 (e.g., node L2 is transparent due to NCK being high), the setup time for such path can be expressed as follows:

$$S_{L1-L2-L4} = (D_{CK\uparrow-L1} + D_{L1-L2} + D_{L2-L4}) - D_{CK\downarrow-L4}$$
 EQ. 2 where:

 $S_{L1-L2-L4}$ = setup time for path L1-L4;

 $D_{CK\uparrow-L1} = riskingrising CK to L1 delay;$

 D_{L1-L2} = longest delay from L1-L2;

 D_{L2-L4} = longest delay form L2-L4; and

 $D_{CK_1-L_4}$ = falling CK to L4 delay (e.g., occurs in cycle 2).

Please replace the paragraph beginning on page 11, line 15, with the following amended paragraph:

At 210, NODE_i is accessed. The subscript "i" denotes an identified identifier for a given node for which method is being implemented. NODE_i thus corresponds to a given node of a circuit design, which for the first iteration of the method corresponds to a starting node. A starting node can be any node at which an input signal can be received for processing. In one embodiment, the method is implemented for a circuit design that includes nodes implemented as latches or other circuitry capable of operating in both transparent and non-transparent states based on clock signals applied to control the nodes. For example, the nodes can be implemented as latches that are clocked by alternating clock signals (e.g., substantially 180° out of phase), such as to enable cycle stealing throughout the circuit design. The nodes can be spaced between blocks of combinational logic for propagating signals through such logic.